

1 WHAT IS CLAIMED IS:

2 1. A frequency shift keyed (FSK) receiver capable of
3 demodulating an incoming transmitted signal comprising:

4 a phase-locked loop for receiving an oscillator
5 reference signal having a frequency F_1 and generating a reference
6 carrier frequency signal having a desired frequency $N_1(F_1)$,
7 wherein N_1 may be a non-integer value, said phase-locked loop
8 comprising:

9 a phase detector having a first input for
10 receiving said oscillator reference signal and a second
11 input; and

12 a frequency divider circuit for dividing an
13 actual frequency of said reference carrier frequency signal
14 by an adjustable integer value N_2 applied to a control
15 input of said frequency divider circuit to thereby generate
16 a feedback signal applied to said second input of said
17 phase detector;

18 a frequency discriminator that receives said incoming
19 transmitted signal and said reference carrier frequency signal
20 and generates a correction signal corresponding to a difference
21 between a center frequency of said incoming transmitted signal
22 and said actual frequency of said reference carrier frequency
23 signal; and

24 a delta-sigma modulator controlled by said correction
25 signal operable to generate a sequence of integers having an
26 average value of $N1$ over a defined time period, wherein said
27 sequence of integers are applied to said control input of said
28 frequency divider circuit.

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1 2. The FSK receiver as set forth in Claim 1 further
2 comprising a subtraction circuit capable of subtracting said
3 correction signal from a nominal carrier frequency value to
4 thereby generate a control frequency signal that controls said
5 delta-sigma modulator.

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1 3. The FSK receiver as set forth in Claim 1 wherein
2 frequency discriminator comprises a first mixer that receives
3 said incoming transmitted signal and said reference carrier
4 frequency signal and generates an intermediate frequency signal
5 having a frequency equal to a difference between said center
6 frequency of said incoming transmitted signal and said actual
7 frequency of said reference carrier frequency signal.

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1 4. The FSK receiver as set forth in Claim 3 wherein
2 frequency discriminator further comprises a signal splitter that
3 splits said intermediate frequency signal into a first child
4 intermediate frequency signal and a second child intermediate
5 frequency signal.

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1 5. The FSK receiver as set forth in Claim 4 wherein
2 frequency discriminator further comprises a delay element that
3 delays said second child intermediate frequency signal by a
4 delay, T.

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1 6. The FSK receiver as set forth in Claim 5 wherein said
2 delay, T, is a substantially equal to a quarter wavelength of
3 said second child intermediate frequency signal.

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1 7. The FSK receiver as set forth in Claim 5 wherein
2 frequency discriminator further comprises a second mixer that
3 receives said first child intermediate frequency signal and said
4 time-delayed second child intermediate frequency signal and
5 generates a DC correction voltage.

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1 8. The FSK receiver as set forth in Claim 7 wherein said
2 frequency discriminator further comprises an analog-to-digital
3 converter that receives said DC correction voltage and outputs
4 said correction signal.

1 9. A method of demodulating a transmitted signal
2 comprising the steps of:

3 mixing the transmitted signal and a reference carrier
4 frequency signal having a desired frequency $N1(F1)$, wherein $N1$
5 may be a non-integer value, produced by a phase-locked loop (PLL)
6 to generate a correction signal corresponding to a difference
7 between a center frequency of the transmitted signal and an
8 actual frequency of the reference carrier frequency signal;

9 in the phase-locked loop (PLL), dividing the actual
10 frequency of the reference carrier frequency signal by an
11 adjustable integer value $N2$ applied to a control input of a
12 frequency divider circuit to generate a PLL feedback signal
13 having a frequency of $(N1/N2)F1$;

14 in the phase-locked loop, comparing the phase of an
15 oscillator reference signal having a frequency $F1$ and the phase
16 of the PLL feedback signal and using the phase difference to
17 control a voltage controlled oscillator generating the reference
18 carrier frequency signal having the desired frequency $N1(F1)$; and

19 using a delta-sigma modulator controlled by the
20 correction signal to generate a sequence of integers having an
21 average value of $N1$ over a defined time period, wherein the
22 sequence of integers are applied to the control input of the
23 frequency divider circuit.

